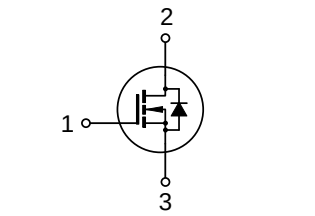
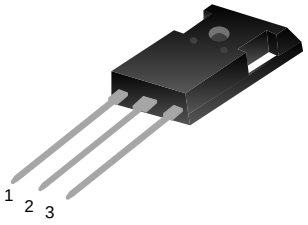
35A, 650V SUPER JUNCTION MOS POWER TRANSISTOR

DESCRIPTION

SVSP35NF65P7D3 is an N-channel enhancement mode high voltage power MOSFETs produced using Silan's DPMOS technology. It achieves low conduction loss and switching losses. It leads the design engineers to their power converters with high efficiency, high power density, and superior thermal behavior. Furthermore, it's universal applicable, i.e., suitable for hard and soft switching topologies.



1.Gate 2.Drain 3.Source



TO-247-3L

FEATURES

- 35A, 650V, $R_{DS(on)(typ.)}$=85mΩ@V_{GS}=10V
- New revolutionary high voltage technology
- Periodic avalanche rated
- Extreme dv/dt rated
- High peak current capability

ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing Type
SVSP35NF65P7D3	TO-247-3L	P35NF65	Halogen free	Tube

ABSOLUTE MAXIMUM RATINGS (UNLESS OTHERWISE NOTED, T_J=25°C)

Characteristics		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DS}	650	V
Gate-Source Voltage		V_{GS}	±30	V
Drain Current	T_C=25°C	I_D	35	A
	T_C=100°C		22	
Drain Current Pulsed(Pulse time 5μs)		I_{DM}	140	A
Power Dissipation (T_C=25°C)		P_D	298	W
- Derate above 25°C			2.4	W/°C
Single Pulsed Avalanche Energy (Note1)		E_{AS}	1131	mJ
Reverse diode dv/dt (Note 2)		dv/dt	50	V/ns
MOSFET dv/dt ruggedness (Note 3)		dv/dt	100	V/ns
Operation Junction Temperature Range		T_J	-55～+150	°C
Storage Temperature Range		T_{stg}	-55～+150	°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Test conditions	Ratings			Unit
			Min.	Typ.	Max.	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	--	--	--	0.42	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	--	--	--	50	°C/W
Soldering Temperature (in line)	Tsold	15^{+2}_{-0} sec, 1time	--	--	260	°C

ELECTRICAL CHARACTERISTICS (UNLESS OTHERWISE NOTED, T_J=25°C)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA	650	--	--	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=650V, V_{GS}=0V, T_J=25°C	--	--	6.0	μA
		V_{DS}=650V, V_{GS}=0V, T_J=125°C	--	80	--	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±30V, V_{DS}=0V	--	--	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=250μA	2.5	--	4.5	V
Static Drain- Source on State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=17.5A	--	85	100	mΩ
Gate resistance	R_g	f=1MHz	--	1.1	--	Ω
Input Capacitance	C_{iss}	V_{DS}=100V, V_{GS}=0V, f=1.0MHz	--	2923	--	pF
Output Capacitance	C_{oss}		--	109	--	
Reverse Transfer Capacitance	C_{rss}		--	20	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=325V, V_{GS}=10V, R_G=1.6Ω, I_D=35A (Note 4,5)	--	28	--	ns
Turn-on Rise Time	t_r		--	69	--	
Turn-off Delay Time	$t_{d(off)}$		--	92	--	
Turn-off Fall Time	t_f		--	28	--	
Total Gate Charge	Q_g	V_{DD}=520V, V_{GS}=10V, I_D=35A (Note 4,5)	--	139	--	nC
Gate-Source Charge	Q_{gs}		--	21	--	
Gate-Drain Charge	Q_{gd}		--	92	--	
Gate-plate voltage	Vplateau		--	7.1	--	V

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	T_C=25°C, Integral Reverse P-N Junction Diode in the MOSFET	--	--	35	A
Pulsed Source Current	I_{SM}		--	--	140	
Diode Forward Voltage	V_{SD}	I_S=35A, V_{GS}=0V	--	--	1.4	V
Reverse Recovery Time	T_{rr}	I_S=35A, V_{GS}=0V, dI_F/dt=100A/μs (Note 4)	--	125	--	ns
Reverse Recovery Charge	Q_{rr}		--	0.6	--	μC
Reverse Recovery Peak Current	Irrm		--	10	--	A

Notes:

1. L=79mH, I_{AS}=5.0A, V_{DD}=100V, R_G=25Ω, starting temperature T_J=25°C;
2. V_{DS}=0~400V, I_{SD}<=35A, T_J=25°C;
3. V_{DS}=0~400V;
4. Pulse Test: Pulse width ≤300μs,Duty cycle≤2%;
5. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

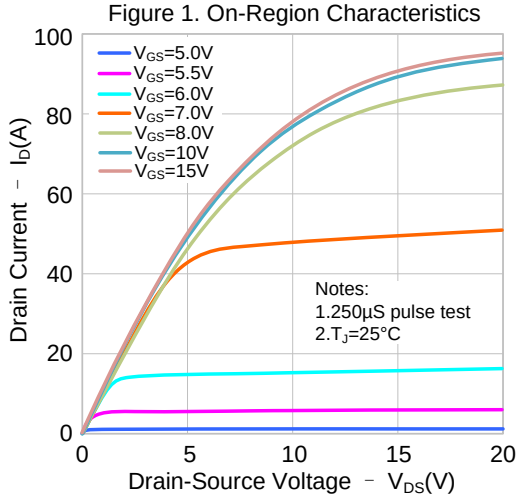


Figure 2. On-Region Characteristics

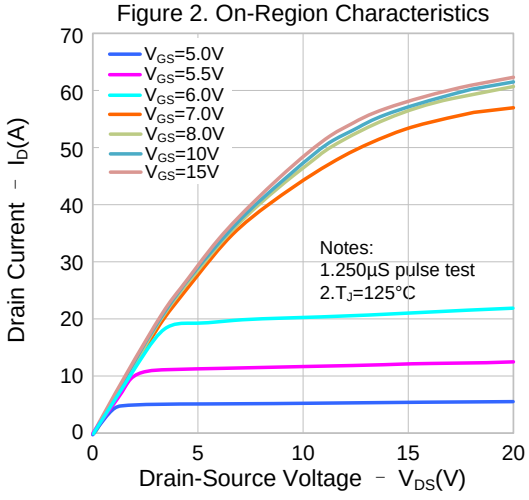


Figure 3. Transfer Characteristics

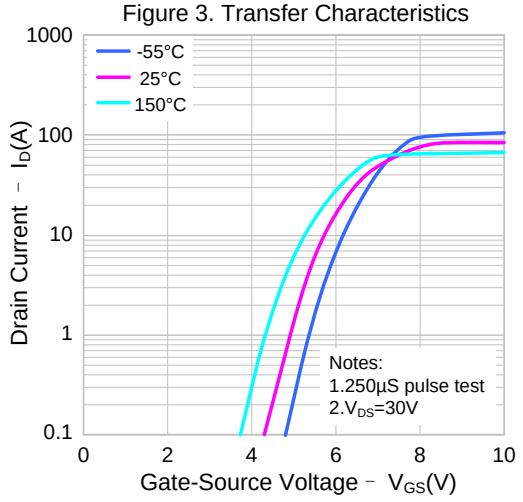


Figure 4. On-Resistance Variation vs. Drain Current

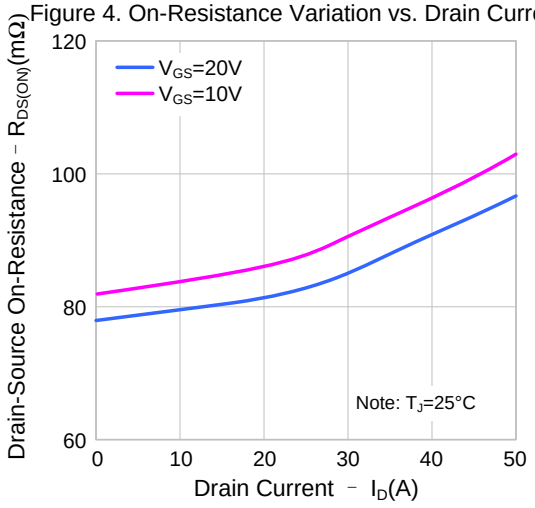


Figure 5. On-Resistance Variation vs. Gate-Source Voltage

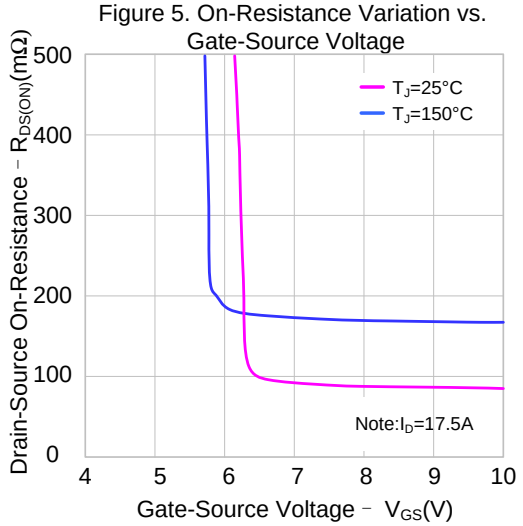
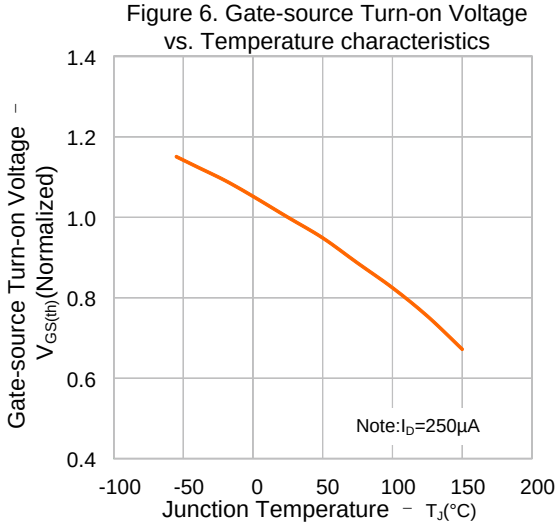


Figure 6. Gate-source Turn-on Voltage vs. Temperature characteristics



TYPICAL CHARACTERISTICS (CONTINUED)

Figure 7. Body Diode Forward Voltage Variation vs. Source Current and Temperature

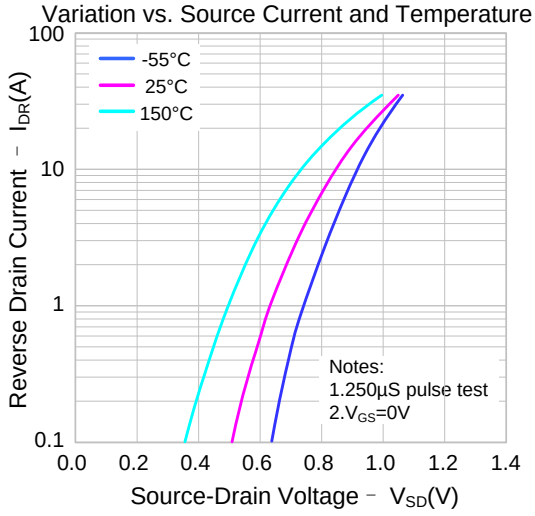


Figure 8. Capacitance Characteristics

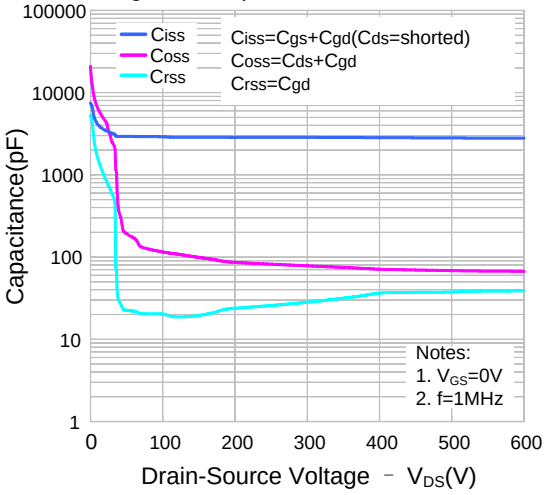


Figure 9. Gate Charge Characteristics

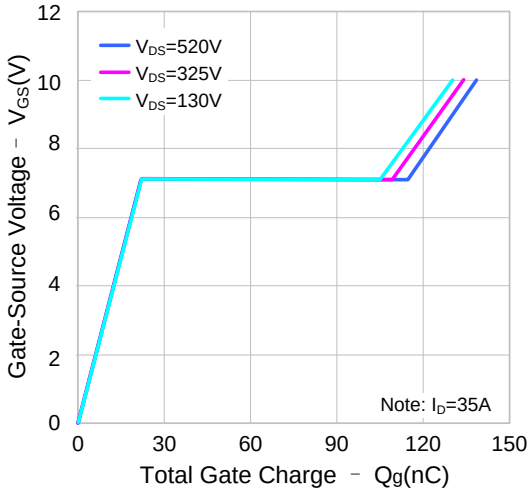


Figure 10. Breakdown Voltage Variation vs. Temperature

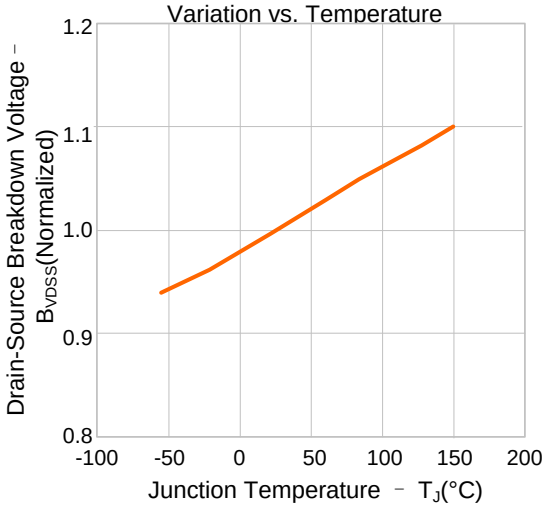


Figure 11. On-resistance Variation vs. Temperature

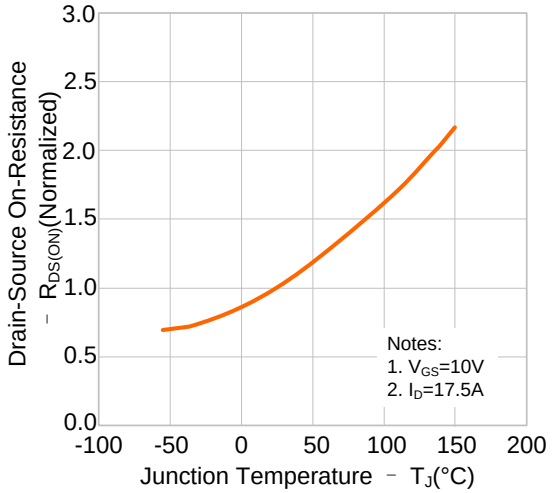
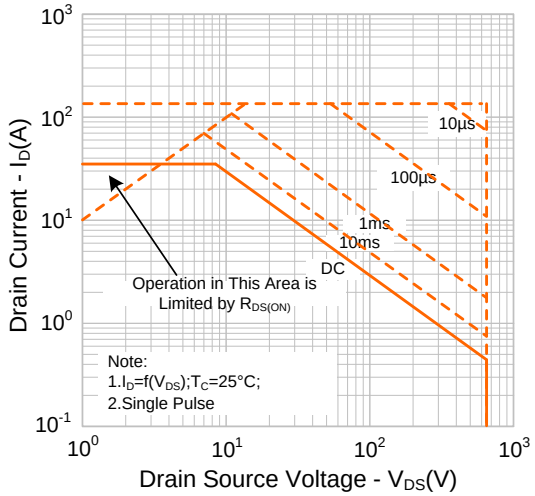


Figure 12. Max. Safe Operating Area



TYPICAL CHARACTERISTICS (CONTINUED)

Figure 13. Power dissipation vs. Case Temperature

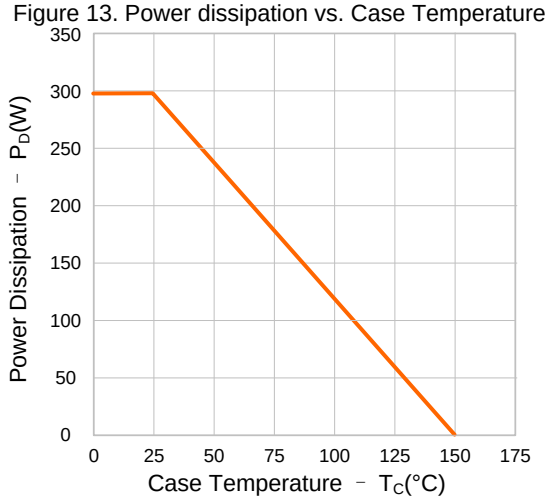


Figure 14. Max. Drain Current vs. Case Temperature

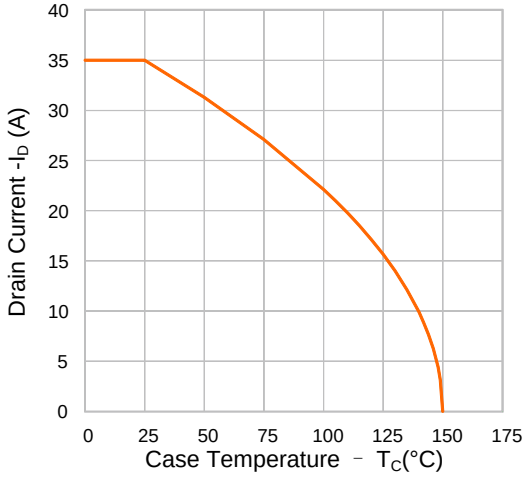
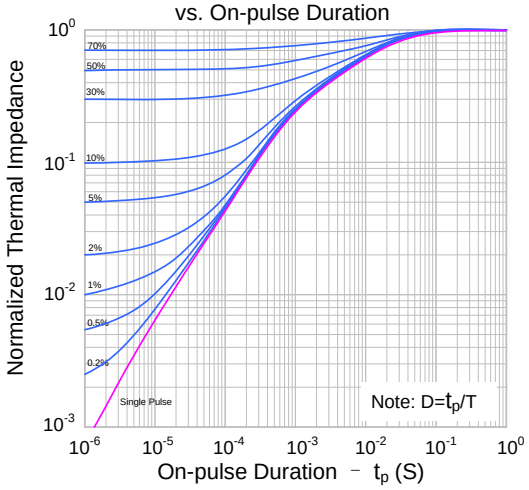
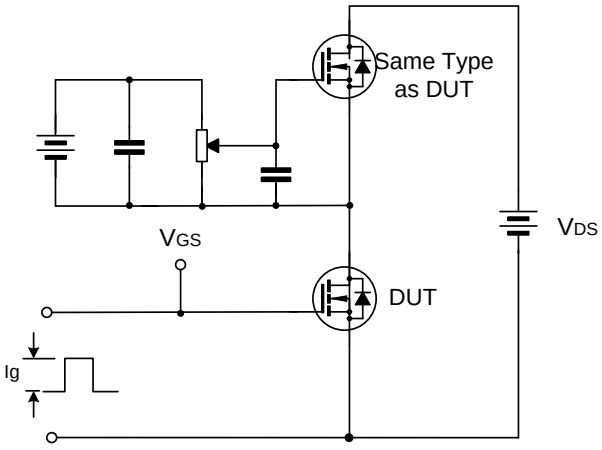


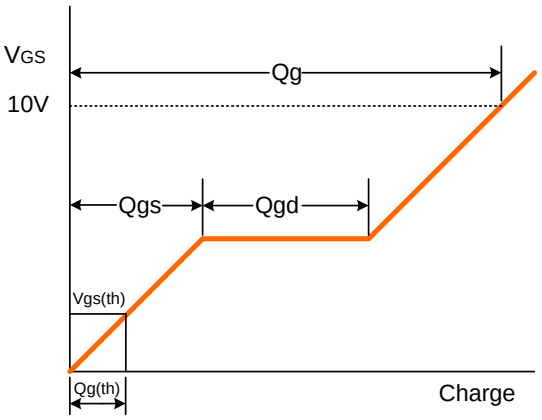
Figure 15. Transient Thermal Impedance vs. On-pulse Duration



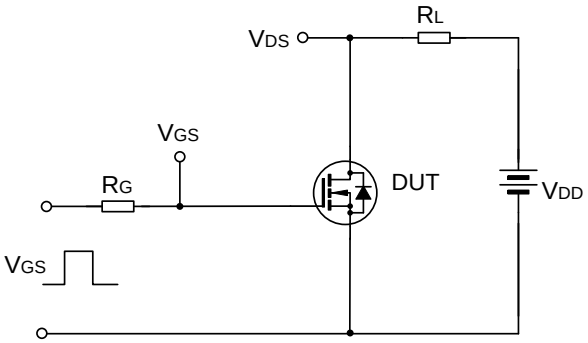
TYPICAL TEST CIRCUIT

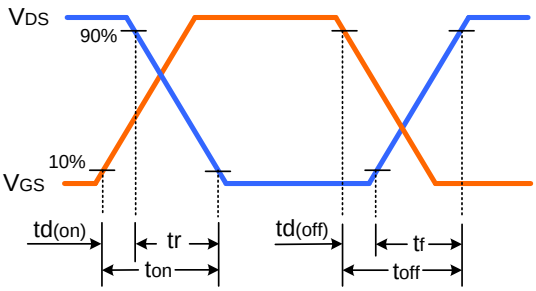
Gate Charge Test Circuit & Waveform



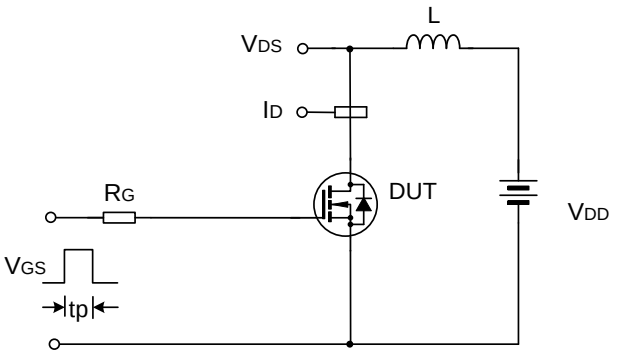


Resistive Switching Test Circuit & Waveform

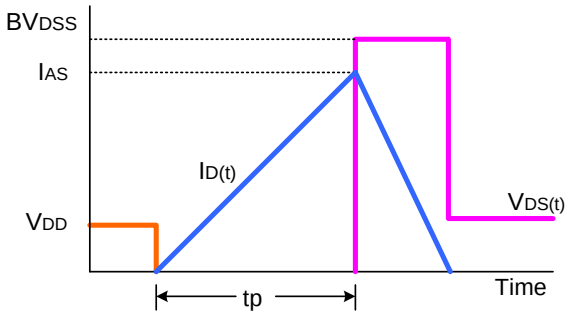




Unclamped Inductive Switching Test Circuit & Waveform

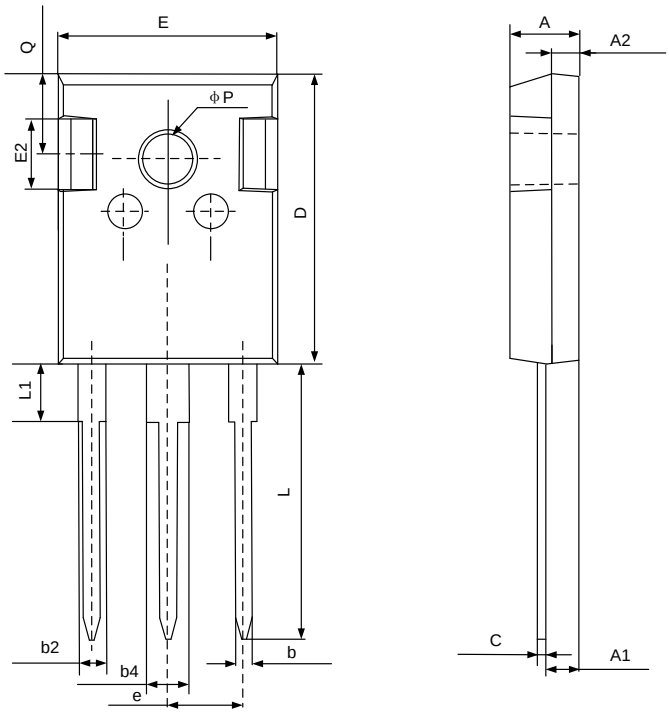


$$E_{AS} = \frac{1}{2} LI_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$



PACKAGE OUTLINE

TO-247-3L **UNIT: mm**



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	4.80	5.00	5.20
A1	2.21	2.41	2.59
A2	1.85	2.00	2.15
b	1.11	–	1.36
b2	1.91	–	2.25
b4	2.91	–	3.25
c	0.51	–	0.75
D	20.80	21.00	21.30
E	15.50	15.80	16.10
E2	4.40	5.00	5.20
e	5.44 BSC		
L	19.72	19.92	20.22
L1	–	–	4.30
Q	5.60	5.80	6.00
P	3.40	—	3.80

Important notice :

1. **The instructions are subject to change without notice!**
2. **Customers should obtain the latest relevant information before placing orders and should verify that such information is complete and current. Please read the instructions carefully before using our products, including the circuit operation precautions.**
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Rev.: 1.2

Revision History:

1. Update figures 6, 12 and 14
2. Add figure 15

Rev.: 1.1

Revision History:

1. Update ELECTRICAL CHARACTERISTICS
2. Update the template of datasheet

Rev.: 1.0

Revision History:

1. First release